POWER AMPLIFIER LINEARIZATION USING DIGITAL PREDISTORTION – SIMULATION AND IMPLEMENTATION

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Abstract

This paper presents our experiments with the power amplifier (PA) linearization using the digital predistortion. The results of MATLAB simulations of digital predistortion are presented. Finally, the first results of DSP implementation resulting from succesfull MATLAB evaluation are briefly discussed.

1 Introduction

The current and future standards of mobile communications and local area networks use the digital modulations with non-constant envelope. For the reasons of higher efficiency, power amplifiers (PA) working in nonlinear regions are widely employed. The nonlinearities present in the power amplifier driven with non-constant envelope signal are at the origin of in-band as well as out-of-band emissions.

In order to allow the use of nonlinear PA together with digital modulation signals with high dynamic, some of the linearization methods is often used. This paper deals with the digital adaptive baseband predistortion, one of the methods that allow to treat the nonlinearity in digital domain and is thus suitable for the implementation on DSP.

In second chapter, the models of PA are described. The third chapter briefly describes the theory of digital baseband adaptive predistortion. Its MATLAB simulation together with the results obtained are presented in chapter 4. Final chapter focus on the implementation of the predistortion algorithm on the digital signal processor TMS320C6711.

2 Power amplifier models

The behavior of a memoryless PA can be completely characterized by its AM/AM and AM/PM curves. These characteristics give the PA output power and phase, respectively, as the functions of PA input power for the case of single-tone PA input signal. The amplifier operator A can thus be described using following equation:

$$A\left(z_n\right) = AM\left(\left|z_n\right|^2\right)\exp(j(\arg(z_n) + PM\left(\left|z_n\right|^2\right))) \tag{1}$$

where *AM, PM* denote the AM/AM and AM/PM characteristics, respectively. The PA input complex envelope is z_n. Although originally proposed for TWT amplifiers, the Saleh model [4] is widely used as the reference for the evaluation of predistortion algorithms. The PA exhibiting memory effects for the wideband signals can be modeled using a polynomial with memory:

$$A(z_n) = \sum_{k=0}^{N-1}\sum_{l=0}^{L} a_{k,l} z_{n-ln_0}\left|z_{n-ln_0}\right|^k \tag{2}$$

where $a_{k,l}$ are the PA model polynomial coefficients, *N* is the order of polynomial and *L* is the memory length.

3 Digital adaptive predistortion

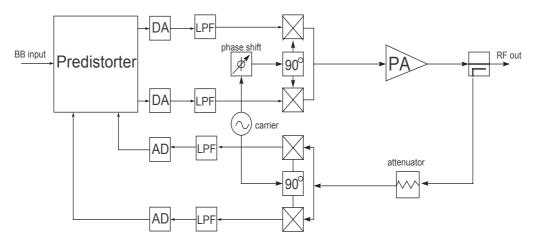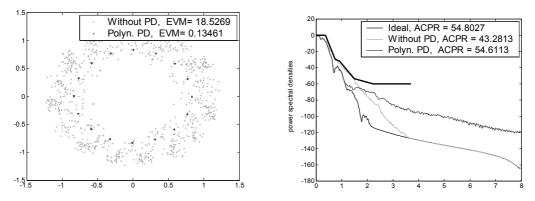The principal schematic of digital adaptive baseband predistortion is shown in figure 1.

Fig. 1 Digital baseband adaptive predistortion principle

The digitally modulated base band (BB) signal is processed by a predistorter, modeling the inverse AM/AM and AM/PM characteristics of the amplifier to linearize. To make the system adaptive, a part of the PA output is downconverted to the baseband and used to adapt the predistorter for the changes in PA characteristics caused by device aging, temperature, etc.
The digital predistorters can be classified into two main groups. The first are the predistorters implemented as a Look Up Table (LUT). Second group are so called parametric predistorters, that are implemented for example as a polynomial function, or a polynomial with memory.

4 MATLAB simulation

The simulation of the predistorter (memoryless as well as employing memory effects having the structure according eq. 2) has been done in MATLAB environment using standard functions and toolboxes. The criteria like power spectra, ACPR, EVM have been regarded to evaluate the predistorters performance. In fig. 2, the example of results for the memoryless polynomial predistorter (special case of predistorter with memory with L=0) applied to the linearization of PA described using Saleh model is presented. The improvement in terms of all above mentioned criteria is evident.

Fig. 2 : Results of MATLAB simulations. Polynomial predistorter for the linearization of Saleh model driven with GSM-EDGE signal. Constellation diagram (left) and power spectral densities (right)

The evolution in time of the polynomial predistorter coefficients has been plotted in fig. 3. Note that all the figures have been obtained from MATLAB.
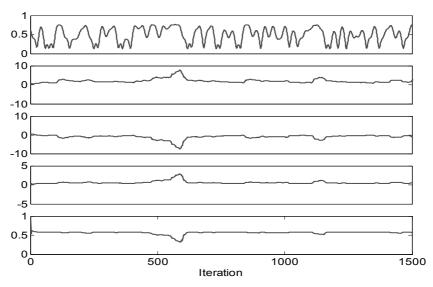
Fig. 3 : Evolution of PD coefficients with number of iterations

5 DSP implementation

A set of the algorithms for the digital predistortion described above is currently subject of the implementation on the family of signal processor TMS320C6000. Our Laboratory of signal processing is equipped with the DSK including a floating point DSP TMS320C6711 running at the frequency 150MHz, [3]. The C6000 is the most powerful family of Texas Instruments DSP's with Very Long Instruction Word architecture. It contains 8 functional units, and up to 8 instructions can thus be run in parallel (resulting to theoretical performance of 1200 MIPS). There are three possibilities to program this DSP. The first, easiest but less performing way is the C language programming. On the contrary, the assembler provides the most-efficient code but at the cost of long development phase. A good compromise between these two alternatives is called linear assembler. The linear assembler allows to write the efficient code using assembly instructions, but user does not take care about the unit allocation, time dependency etc.

After the successful MATLAB simulations, we have implemented the polynomial predistorter with or without memory using a C language, without and with the compiler optimization. The parameters of the predistorter have been chosen to N=6 and L=1, conducting to 12 predistorters coefficients. Although the highest compiler optimization (–o3) has been turned on, calculation of one sample needed approximately 7000 cycles.

Subsequently, in order to speed up the execution, the code has been rewritten into linear assembly. Several modifications of the basic algorithm have been examined. The number of cycles needed for one sample calculation has been reduced to 1880 by pure rewriting from C into linear assembly. Further effort resulted in another cycle number reduction to value 620. It is necessary to say that the significant part of this number is due to the built-in sqrt function and the number of cycles will be smaller for memoryless predistorter according [1].

6 Conclusions

A principle of the digital predistortion method for power amplifier linearization has been described in this paper. MATLAB environment appeared to be very convenient for the evaluation of this algorithm and the simulations done in this environment have been a good starting point towards a successful DSP implementation.

Acknowledgement

References

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